## REMARKS

Applicant is in receipt of the Final Action mailed June 2, 2006. Claims 1-64 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

## Objection to the Specification:

Applicants note that while the Examiner's previous objection to the title of the application continues to appear in the body of the instant Final Action, the Examiner has withdrawn the objection in the "Response to Arguments" section of the Final Action.

## Section 102(b) Rejection:

Claims 1-64 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wilkinson et al. (U.S. Patent No. 5,805,915) (hereinafter, "Wilkinson"). Applicants traverse this rejection and submit that claims 1-64 are not anticipated by, or rendered obvious by, Wilkinson, as set forth in greater detail below along with Applicants' responses to the Examiner's additional remarks in the Final Action.

As previously argued with respect to claim 1, Wilkinson fails to teach or suggest all of the limitations of Applicants' claim. Specifically, Wilkinson fails to teach or suggest a plurality of dynamically configurable communication elements, each comprising a plurality of communication ports, a first memory, and a routing engine, wherein the plurality of dynamically configurable communication elements are coupled together with a plurality of processors in an interspersed arrangement. Wilkinson further fails to teach or suggest that for each of the processors, a plurality of included processor ports are configured for coupling to a first subset of the plurality of dynamically configurable communication elements, and that for each of the dynamically configurable communication elements, the plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of the plurality of the processors

and a second subset of communication ports configured for coupling to a second subset of the plurality of dynamically configurable communication elements.

As shown in Figures 2 and 4, Wilkinson teaches only a uniform array of interconnected picket processors 100, not an interspersed array of processors and communication elements as recited in claim 1. The Examiner relies on Wilkinson, col. 23, lines 11-16 in asserting that DCC elements are "part of the picket array" of Wilkinson, pointing to col. 22, lines 30-67 in asserting that Wilkinson discloses the communication ports and memory features of the DCC elements of claim 1. Essentially, the Examiner is attempting to argue that each picket 100 of Wilkinson corresponds to both a processor and a communication element of claim 1. However, this interpretation renders the remainder of claim 1 incoherent, in that claim 1 requires that DCC elements have a first subset of communication ports configured for coupling to processors and a second subset of communication ports configured for coupling to other DCC elements. In attempting to show that Wilkinson satisfies this arrangement of connectivity, the Examiner refers to I/O ports 520 discussed at col. 22, lines 30-56 and col. 23, lines 1-16. However, I/O ports 520 have nothing to do with interfacing individual pickets 100 with one another. Rather, Wilkinson clearly discloses that these ports are configured for "communication to associated mainframes or otherwise to the rest of the world," (col. 22, lines 55-56) that is, for communication not among, but external to pickets 100.

Claim 1 requires that a processor including an ALU and an instruction processing unit be configured for coupling, via processor ports, to a subset of DCC elements each including a memory and a routing engine, where DCC elements in turn include ports configured for coupling to processors and other DCC elements. By contrast, Wilkinson discloses a plurality of pickets 100, each including its own memory 102, and each passively connected to one another via propagate and broadcast buses (as shown in Figure 2). Further, while claim 1 clearly requires that DCC elements include a routing engine, it is not clear from the disclosure of Wilkinson that any routing of communications is performed by the pickets themselves. Rather, Wilkinson clearly discloses that execution control of and communication among pickets 100 is controlled

by instruction sequencer 402 and execution control 403, which are entirely distinct from and not interspersed among pickets 100 (Figure 4 and col. 20, lines 4-30).

Applicants note that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As Wilkinson discloses dissimilar elements arranged in a fundamentally different fashion compared to Applicants' claim 1, Wilkinson cannot be said to anticipate claim 1.

In the "Response to Arguments" section of the Final Action, the Examiner asserts that "[n]owhere in Wilkinson is the array described as uniform," "Figures 2 and 4 are not enough evidence to prove uniformity," and "applicant did not clearly define the term interspersed and thus the broadest interpretation of the term (to place at intervals) was used."

Applicants traverse these remarks. Wilkinson provides a comprehensive glossary of terms in cols. 1-7 in which he defines a hardware array as "a collection of structures (functional elements) which are generally identical in a massively parallel architecture... Generally arrays may be thought of as grids of processing elements." (col. 2, lines 7-14, emphasis added) Wilkinson further defines a picket array as "...a collection of pickets arranged in a geometric order, a regular array" (col. 6, lines 16-17, emphasis added) and a picket as "...the element in an array of elements making up an array processor... The term PICKET is similar to the commonly used array term PE for processing element, and is an element of the processing array preferably comprised of a combined processing element and local memory..." (col. 5, lines 47-60, emphasis added).

It is clear from Wilkinson's definitions and embodiments shown in Figures 2 and 4 that Wilkinson discloses an array of pickets that are generally identical. Further, as

Applicants previously noted and as further supported by the definitions cited above, Wilkinson specifically teaches that each such picket includes both a processing element and a memory that is local to that processing element.

Applicants note that claim 1 does not merely recite "an interspersed array." Rather, claim 1 recites that a plurality of processors and a plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement. Wilkinson discloses a completely different system topology in which pickets are coupled together in a regular array. Wilkinson fails to disclose any sort of element resembling Applicants' recited dynamically configurable communication element that is interspersed among the pickets as required by claim 1. In fact, as shown in Figures 2 and 4, Wilkinson discloses identically-configured pickets 100 directly coupled to one another.

As argued above, Wilkinson additionally fails to disclose the specific configuration of ports of each dynamically configurable communication element as required by claim 1. To reiterate, claim 1 requires that for each of the dynamically configurable communication elements, the plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of the plurality of the processors and a second subset of communication ports configured for coupling to a second subset of the plurality of dynamically configurable communication elements.

In the "Response to Arguments" section of the Final Action, the Examiner makes a general reference to Wilkinson as disclosing communication among pickets, and infers that such communication necessarily implies that Wilkinson includes communication elements and ports. Applicants traverse the Examiner's remarks. First, claim 1 does not merely recite communication elements, but rather communication elements distinct from and coupled together with processing elements in an interspersed arrangement. Merely identifying a feature in Wilkinson that could potentially be used for communication does not satisfy all of the limitations of the communication element as recited in claim 1. Moreover, merely inferring that communication among pickets requires some sort of port

does not amount in any way to a disclosure of how those ports are configured as recited in claim 1. That is, claim 1 recites specific limitations as to how communication ports of the dynamically configurable communication element are configured for coupling to subsets of both the recited processors and other ones of the recited communication elements. The fact that Wilkinson does not disclose the basic configuration of elements required by claim 1 renders it impossible for Wilkinson to disclose the specific manner in which those elements are interconnected. Applicants note once again that anticipation requires not only a complete disclosure of every element in a claim, but a complete disclosure of the claimed relationships among those elements.

As argued above, Wilkinson fails to teach or suggest that dynamically configurable communication elements, coupled together with processors in an interspersed arrangement, each includes a routing engine. In the "Response to Arguments" section of the Final Action, the Examiner acknowledges that Wilkinson does not explicitly teach a routing engine, but asserts that because Wilkinson discusses routing in general, a routing engine is necessarily implied. Applicants traverse these remarks and remind the Examiner that the mere inference of a feature resembling a claimed element does not amount to a complete disclosure of the element as claimed. In claim 1, it is specifically required that the routing engine be included within a dynamically configurable communication element. Notwithstanding the fact that Wilkinson fails to teach this element as fully required by claim 1, Wilkinson fails to ascribe routing functionality to any element actually within the picket array, instead providing a control bus to pickets 100 from execution control 403 residing external to the picket array (Figure 4 and col. 20, lines 4-24).

For at least the foregoing reasons, Applicants submit that the Examiner's rejection of claim 1 is in error, and that claim 1 is clearly distinguishable over the cited art.

Applicants also note that Wilkinson fails to teach or suggest the limitations recited in claim 64. Specifically, Wilkinson fails to teach or suggest that for at least one of the plurality of dynamically configurable communication elements, the first memory includes

a plurality of addressable locations and is configured to substantially simultaneously provide a plurality of values stored in the plurality of addressable locations to two or more of the processors. Instead, Wilkinson provides each picket processor 100 with its own respective memory 102, and makes no suggestion whatsoever that a given memory 102 provides data to any entity other than the ALU 101 of the picket 100 in which the given memory 102 is included (Figure 2 and col. 19, lines 50-60). Thus, Applicants submit that claim 64 is distinguishable over Wilkinson.

In the "Response to Arguments" section of the Final Action, the Examiner makes a general assertion that Wilkinson discloses the sharing of data among pickets 100. However, Applicants note that claim 64 does not recite the mere sharing of data, but requires that a memory included within one of the dynamically configurable communication elements is configured to substantially simultaneously provide stored values to two different processors. Applicants submit that Wilkinson does not disclose or suggest any aspect of a memory that is so configured.

Wilkinson further fails to teach or suggest the limitations of independent claim 41. First, as argued above with respect to claim 1, Wilkinson fails to teach or suggest the arrangement of processors and communication elements recited in claim 41. Further, Wilkinson fails to teach or suggest that one of the processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of the plurality of dynamically configurable communication elements to a destination device, wherein, after the source device begins transfer of the first plurality of data through the intermediate subset to the destination device, if either the destination device or one of the intermediate subset stalls, the stalling device is operable to propagate stalling information through one or more of the intermediate subset to the source device, and wherein the source device is operable to suspend transfer of the first plurality of data upon receipt of the stalling information, wherein a portion of the first plurality of data transmitted after the stalling and prior to the suspending is buffered in at least one of the intermediate subset.

The Examiner relies upon col. 19, lines 10-20 of Wilkinson to demonstrate that Wilkinson discloses the stalling behavior recited in claim 41. However, the cited portion of Wilkinson has nothing whatsoever to do with detecting or propagating stall behavior information, or responding to such information in any way. The cited portion refers to a particular example application of Wilkinson's system in which each picket 100 is assigned to model a particular gate or logic function of a digital system (col. 18, lines 62-65). In particular, Wilkinson discloses broadcasting a name and value of a modeled signal to all pickets 100 in response to the modeled signal changing value, whereupon pickets 100 assigned to model gates having input signal names that match the broadcast name receive the changed value and accordingly modify the computed values of the gates (col. 19, lines 1-14). However, the broadcast information is not stalling information; in fact, it does not indicate anything about the operational status of a processor or DCC element at all. Rather, it is information indicative of the value of a logic signal modeled by a picket. Further, upon receipt of a broadcast signal name, Wilkinson does not suspend transfer of data. Rather, Wilkinson uses the receipt of a signal name as a trigger to capture the value associated with the signal name. As neither the cited portion nor any other portion of Wilkinson disclose the data transfer stalling behavior recited in claim 41, Wilkinson cannot anticipate claim 41. Similar arguments apply to independent claims 43, 45 and 49, each of which recites limitations pertaining to stalling information.

In the "Response to Arguments" section of the Final Action, with respect to the limitation of claim 41 that one of the processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of the plurality of dynamically configurable communication elements to a destination device, the Examiner asserts that col. 23, lines 1-5 of Wilkinson disclose this limitation. Applicants traverse the Examiner's remarks. The cited portion of Wilkinson was referenced by the Examiner to address the limitation of claim 1 wherein dynamically configurable communication elements include routing engines. As argued above, this portion of Wilkinson discusses the concept of routing in general and does not disclose any details of how such routing may be implemented within Wilkinson's picket array. As argued above with respect to

claim 1, Wilkinson simply does not teach the topology of processors and dynamically configurable communication elements as recited in claim 41.

With respect to Applicants' arguments regarding the limitations of claim 41 pertaining to stalling feature, the Examiner reiterates the reference to col. 19, lines 10-20 of Wilkinson and asserts that "[w]hen a process is run in parallel, and a signal change is done, a stall is implied as the process must be suspended in order to implement this change. The signal change is the manner in which a stall is propagated. Thus all operations of the stall device is [sic] disclosed..."

Applicants traverse the Examiner's comments. Once again, the cited portion of Wilkinson refers to a particular computational application of Wilkinson's picket processor for use in modeling logic elements of a VLSI system under design. Nowhere in this section nor elsewhere within the reference does Wilkinson disclose the specific details of stalling and suspension of data transfer as recited in claim 41. Moreover, the Examiner's interpretation of how the described application of Wilkinson's array actually operates is simply incorrect. The Examiner asserts that when a signal change of a modeled logic element changes, "a stall is implied." But Wilkinson makes no suggestion of this whatsoever.

The cited portion of Wilkinson reads as follows:

> Each time a signal changes, its name is broadcast on bus 103 to all pickets and this name is compared in parallel with the names of expected input signals. If a match is found, a subsequent step records in the picket a new value of the signal in a dataflow register bit. When all signal changes have been recorded, such an enhanced process would cause all pickets to read out in parallel a control word which tells their data flow how to use the current set of inputs to compute the output. The process would then cause these computations to be performed in parallel, with the results compared with the old value from the local gate. Subsequently the improved process should record as a dataflow status bit all of those gates of the pickets whose outputs change. Then, the process would cause an external controller to interrogate all the pickets and ask for the next gate that changed. Then, the system would be caused to broadcast the appropriate

signal name and value from the picket to all other pickets, as originally stated, and repeat the cycle until no more signal changes occur or until the process is stopped.

In this portion, Wilkinson discloses that pickets compare modeled signal inputs to names of expected input signals to detect signal changes. If a modeled signal input does change, a picket captures a new value of the signal, and subsequently computes a new output value for the output signal modeled by the picket, to be broadcast as a new signal value to the other pickets. Far from stalling when a modeled signal changes, it is clear from Wilkinson that the pickets must be active, as it is the activity of the pickets that implements the modeled behavior of the signal changes in the first place. That is, in Wilkinson, a modeled signal change is the collection of active behaviors implemented by pickets 100 in receiving notice of the change and computing new output values reflective of the change. It is hardly essential, contrary to the Examiner's suggestion, that the pickets must stall in order to implement this process. If anything, Wilkinson suggests completely the opposite – that is, that the pickets must operate continuously to implement this process.

Wilkinson further fails to teach or suggest the limitations of independent claim 52. As argued above with respect to claim 1, Wilkinson fails to teach or suggest processors and dynamically configured communication elements coupled together in an interspersed arrangement. Additionally, Wilkinson fails to teach or suggest that the processors and DCC elements are manufactured on a single integrated circuit, and that each DCC element includes input ports, output registers, and a crossbar, wherein each of the output registers selectively operates in a synchronous data transfer mode or a transparent data transfer mode.

In asserting that Wilkinson teaches that processors and DCC elements are manufactured on a single integrated circuit, the Examiner refers to col. 18, line 56, which refers to one application of the picket system in implementing "checkers for VLSI ground rules violations." However, this refers to a use of Wilkinson's system, and has nothing whatsoever to do with how the system is implemented. In fact, in Figure 5 and at col. 22,

lines 6-62, Wilkinson discloses that the picket system is implemented on distinct cards implemented within a rack-mount system, which is precisely the opposite of manufacturing the system on a single integrated circuit.

To support the assertion that Wilkinson discloses that DCC element output registers selectively operate in a synchronous or transparent data transfer mode, the Examiner refers to col. 8, line 64 – col. 9, line 6. However, the referenced section refers broadly to an array processor embodiment in which processors may execute independently of one another and may be synchronized with one another prior to sharing data with one another. Synchronizing independently executing processors simply has nothing to do with a register that selectively operates in a synchronous or transparent data transfer mode.

For at least these reasons, Wilkinson fails to anticipate claim 52. Similar arguments also apply to independent claims 56, 57 and 61, which also recite features relating to devices that operate in a synchronous or transparent data transfer mode. Applicants note that in rejecting claims 57 and 61, the Examiner once again refers to col. 19, lines 10-20, this time asserting that this passage discloses various aspects of synchronous and transparent data transfer recited in Applicants' claims. However, as argued above with respect to claim 41, this section of Wilkinson describes a particular logic circuit modeling application of the picket processor system. It simply has nothing whatsoever to do with data transfer stalling or synchronous or transparent data communication among processors or communication elements.

In the "Response to Arguments" section of the Final Action, the Examiner asserts that in the broadest interpretation of the term, "cards are integrated circuits." Applicants traverse the Examiner's remark and note that, according to MPEP 2111, claims must be given their broadest reasonable interpretation consistent with the specification, and further that the interpretation applied must be consistent with the interpretation those skilled in the art would reach. Applicants submit that the Examiner's suggested interpretation is neither reasonable in view of Applicants' specification nor consistent

with the interpretation of those of skill in the computer arts. That is, one of skill in the computer arts would recognize that a card may include numerous integrated circuits, but that the card itself is distinct from any of the integrated circuits located thereon. Wilkinson's disclosure includes numerous examples of this terminological distinction, referring to both a "chip" or integrated circuit and the cards on which the chips may reside.

With respect to Applicants' assertion that Wilkinson fails to teach or suggest selective operation of output registers in either a synchronous or transparent data transfer mode, the Examiner acknowledges within the "Response to Arguments" section of the Final Action that the original interpretation of the claim was incorrect but refers to col. 23, lines 1-5 and 20-31, asserting that "[d]ata transfers between registers have been established and normal operation works on a common sequencer with clocks and pickets are synchronized [sic], thus normal operations (like data transfers) would be clocked." Further, the Examiner asserts that "[a] transparent data transfer mode could be the broadcasts disclosed on column 21, lines 4-6. A broadcast does not need to be timed and thus could be asynchronous."

Applicants traverse the Examiner's remarks. With regard to the Examiner's first assertion, Applicants note that the referenced portion of Wilkinson discloses that pickets may be synchronized to a common clock signal. However, this does not amount to an assertion that all operational features of pickets are synchronous, and specifically neither teaches nor suggests that an output register of a dynamically configurable communication element may be configured to operate in a synchronous mode. As argued above with respect to claim 1, Wilkinson fails to disclose the broad features of processors and dynamically configurable communication elements coupled together in an interspersed arrangement as required by claim 52, much less the specific structural details of the dynamically configurable communications elements as recited therein. With regard to the Examiner's second assertion, Applicant notes that mere speculation by the Examiner as to how a broadcast operation might or might not operate does not amount to a teaching

grounded in the art. Aside from defining the term "asynchronous," Wilkinson is silent as to what, if any operations of the picket array are in fact asynchronous.

Wilkinson further fails to teach or suggest the limitations of independent claim 62. As argued above with respect to claim 1, Wilkinson fails to disclose processors and dynamically configurable communication elements configured for coupling as recited in claim 62. Moreover, as argued above with respect to claim 52, Wilkinson does not disclose any aspect of manufacturing such processors and communication elements as an integrated circuit, including fabricating, placing and interconnecting units each comprising a processor and a communication element on a substrate. In fact, as argued above, Wilkinson explicitly discloses that the picket processing system is implemented via discrete components on processor cards within a rack-mount system, which is precisely contrary to manufacturing of system components on a single substrate as an integrated circuit. Thus, Wilkinson fails to anticipate claim 62.

Wilkinson further fails to teach or suggest the limitations of independent claim 63. As argued above with respect to claims 1 and 62, Wilkinson fails to disclose processors and dynamically configurable communication elements configured for interrelated coupling and manufactured on a single integrated circuit as recited in claim 63. Claim 63 additionally recites that each communication element includes a routing engine configured to route data between any of the communication ports of the communication element, and a direct memory access engine coupled to the communication ports and configured to transfer data between a memory of the communication element and the communication ports.

In rejecting claim 63, the Examiner asserts that col. 15, lines 5-7 and col. 18, lines 7-18 disclose the routing engine and DMA engine features. However, col. 15 merely refers to the distribution of memory among the nodes of a prior art system that is not Wilkinson's embodiment. This has nothing to do with a routing engine configured to route data among ports, and does not amount to a disclosure of a DMA engine of a communication element as recited in Applicants' claim. Even if it did, as argued above

with respect to claim 52, a proposed combination of the prior art embodiment with Wilkinson's embodiment could not be said to anticipate claim 63. The cited portion of col. 18 merely refers to an associative memory, which has nothing to do with a DMA engine. Thus, Wilkinson fails to anticipate claim 63.

Applicants further submit that the present claims are not obvious in view of Wilkinson based on the arguments cited above. Applicants additionally note that numerous ones of the dependent claims recite additional distinctions over the cited art. However, as each of the independent claims has been shown to be distinguishable, further discussion of the dependent claims is unnecessary at this time.

## CONCLUSION

In light of the foregoing remarks, Applicants submit the application is now in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5860-00101/JCH.

Also enclosed herewith are the following items:

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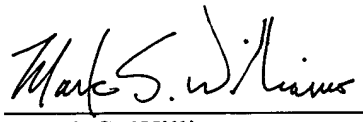
Respectfully submitted,



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